

This listing of the claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently amended) A method of forming a microelectronic structure comprising:

providing a substrate comprising source/drain and gate regions,

wherein the gate region comprises a metal ~~layer~~ gate disposed on a high k

gate dielectric layer, and

laser annealing the substrate.

2. (Currently amended) The method of claim 1 ~~wherein providing a substrate comprising source/drain and gate regions, wherein the gate region comprises a metal layer disposed on a gate dielectric layer comprising providing a substrate comprising source/drain and gate regions, wherein the gate region comprises a~~ further comprising wherein the metal layer comprising gate comprises a work function from about 3.9 electron volts to about 5.2 electron volts that is disposed on the gate dielectric layer.

3. (Currently amended) The method of claim 1 ~~wherein providing a substrate comprising source/drain and gate regions, wherein the gate region comprises a metal layer disposed on a gate dielectric layer further comprises~~ comprising wherein the metal ~~layer~~ gate does not substantially diffuse into the high k gate dielectric layer.

4. (Currently amended) The method of claim 1 ~~wherein providing a substrate comprising source/drain and gate regions, wherein the gate region comprises a metal layer disposed on a gate dielectric layer further comprises~~ comprising wherein the metal layer ~~gate~~ does not substantially diffuse into a polysilicon layer disposed on the metal layer gate.
5. (Currently amended) The method of claim 1 wherein laser annealing the substrate comprises exposing the substrate to a laser beam for a time sufficient to activate an implanted species.
6. (Original) The method of claim 1 wherein laser annealing the substrate comprises exposing the substrate to a laser beam pulsed at about 20 nanosecond intervals or less.
7. (Original) The method of claim 1 wherein laser annealing the substrate comprises activating an implanted species in the source/drain regions by laser annealing.
8. (Currently amended) The method of claim 7 ~~wherein activating an implanted species in the source/drain regions by laser annealing comprises activating an implanted species in the source/drain regions, further comprising~~ wherein the ratio of the depth of the source/drain regions to the length of the source/drain regions is less than about 1:2 ~~by laser annealing~~.

9. (Canceled)
10. (Currently amended) The method of claim 1 ~~wherein providing a substrate comprising source/drain and gate regions, wherein the gate region comprises a metal layer~~
~~comprises providing a substrate comprising source/drain and gate regions, wherein the gate~~
~~region comprises a further comprising wherein the metal layer gate is~~ selected from the group consisting of tungsten, platinum, ruthenium, palladium, molybdenum and niobium, and their alloys, metal carbides, metal nitrides, metal carbides and conductive metal oxides.
11. (Currently amended) A method of forming a microelectronic structure comprising;
providing a substrate comprising doped source/drain and gate regions,
wherein the gate region comprises a metal layer ~~gate~~ disposed on a high k dielectric layer, and wherein the metal layer ~~gate~~ comprises a work function approximately equal to a work function of n doped polysilicon; and
forming shallow source/drain regions by laser annealing the substrate.
12. (Original) The method of claim 11 wherein forming shallow source/drain regions comprises forming source/drain regions wherein the ratio of the depth of the source/drain regions to the length of the source/drain regions is less than about 1:2.
13. (Currently amended) The method of claim 11 ~~wherein providing a substrate~~

~~comprising doped source/drain and gate regions, wherein the gate region comprises a metal layer disposed on a high k dielectric layer, and wherein the metal layer comprises a work function approximately equal to a work function of n doped polysilicon comprises providing a substrate comprising doped source/drain and gate regions, wherein the gate region comprises a metal layer disposed on a high k dielectric layer, and further comprising wherein the metal layer~~ gate ~~comprises a work function from about 3.9 to about 4.2 electron volts.~~

14. (Currently amended) The method of claim 11 ~~wherein providing a substrate comprising doped source/drain and gate regions, wherein the gate region comprises a metal layer disposed on a high k dielectric layer, and wherein the metal layer comprises a work function approximately equal to a work function of n doped polysilicon comprises providing a substrate comprising doped source/drain and gate regions, wherein the gate region comprises a metal layer disposed on a high k dielectric layer, and further comprising wherein the metal layer~~ gate ~~comprises a work function approximately equal to a work function of p doped polysilicon.~~

15. (Currently amended) The method of claim 11 ~~wherein providing a substrate comprising doped source/drain and gate regions, wherein the gate region comprises a metal layer disposed on a high k dielectric layer, and wherein the metal layer comprises a work function approximately equal to a work function of p doped polysilicon comprises providing a substrate comprising doped source/drain and gate regions, wherein the gate region~~

~~comprises a metal layer disposed on a high k dielectric layer, and further comprising~~ wherein the metal layer gate comprises a work function ~~comprises a work function~~ from about 4.8 to about 5.1 electron volts.

16. (Currently amended) The method of claim 11 ~~wherein providing a substrate comprising doped source/drain and gate regions, wherein the gate region comprises a metal layer disposed on a high k dielectric layer comprises providing a substrate comprising doped source/drain and gate regions, wherein the gate region comprises a metal layer disposed on a~~ further comprising wherein the high k dielectric layer selected from the group consisting of hafnium oxide, zirconium oxide, titanium oxide, and aluminum oxide and /or combinations thereof.

Claims 17-24 (Canceled).